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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/753,673	01/07/2004	I-Sheng Liu	M-15281 US	6785

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EXAMINER	
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ART UNIT	**PAPER NUMBER**
3663	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/753,673	LIU ET AL.	
	Examiner	Art Unit	
	Johannes P. Mondt	3663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 and 3-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Amendment filed 8/20/07 correcting informalities in amendment filed 11/13/06 together with the latter amendment filed 11/13/07 together form the basis for this Office Action. In said Amendments applicant amended claim 1. Comments on Remarks are included below under "Response to Arguments"

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

1. ***Claims 1, 3 and 6-9*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al (5,912,842) in view of Dejenfelt et al (5,914,514).

Chang et al teach a two-transistor PMOS memory cell (cf. title and abstract, first sentence), comprising: a PMOS select transistor 40b (col. 4, l. 2 and Figure 3) having a drain and source 50 and 48, resp. (cf. col. 4, l. 3-7), formed as separate P+ diffusion regions in an N- well 42 (col. 4, l. 2); a PMOS floating gate transistor 40a (col. 4, l. 1) having a drain and a source 46 and 48 (cf. col. 4, l. 6-9) formed as separate P+ diffusion regions in the N- well, wherein the P+ diffusion region 48 that forms the floating gate transistor's drain is the same P+ diffusion region that forms the select gate transistor's source (col. 4, l. 4-6).

Chang et al do not necessarily teach the limitation of an N implant underlying the P+ diffusion region that forms the floating gate transistors' drain with lateral extent substantially the same as a lateral extent of the P+ diffusion region that forms the floating gate transistor's drain.

However, it would have been obvious to teach said limitation in view of Dejenfelt et al, who, in a patent on suppressing punch through a two-transistor cell with select gate and floating gate (title, abstract and "Background of the Invention"), hence art analogous to Chang et al, teach (see Figure 5, col. 4, l. 2+, but also Figures 8 and explanation there, especially col. 6, l. 44+) a high substrate doping of conductivity type opposite to that of said common source / drain 510 (see also 811) underneath the source/drain 407 (col. 4, l. 2) (see also 810) common to a select (access transistor) gate 401A (col. 3, l. 56-57) (see also 805A) and a floating gate 403 (col. 3, l. 58) (see also 805) in said two-transistor cell to avoid punch-through and erasure problems by diminishing the dependence of the access gate on the condition of the floating gate (col.

2, l. 22-51). Said high substrate doping meets the limitation on N implant after correction so as to switch overall all N-type and P-type conductivities (the transistors by Dejenfelt et al are N-channel transistors, in Chang et al they are P-type transistors, while examiner takes official notice that an overall interchanging of P-type and N-type conductivity does not by itself carry any patentable weight in the semiconductor art; It is noted that the ranges for the Arsenic and Boron implants producing the common drain / source and the high substrate implant imply the limitation on substantially the same lateral extent for said N to be met, as also transpires from the Figures (5 and 8).

On claim 3: the drain of the PMOS select transistor in Chang et al 50 couples to a bit line BL0 of a memory array 70 (cf. col. 5, l. 1-15) and a select gate 40b of the PMOS select transistor couples to a word line WL0 (lco.cit.) of the memory array.

On claim 6: the memory cell is configured such that the floating gate transistor is capable of being programmed using band-to-band tunneling because a thin tunnel oxide layer 56 (col. 7, l. 14-33) is included while the two transistors are same type, PMOS, transistors. Furthermore, in reference to the claim language "may be programmed", intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim, with reference to previously cited case law.

On claim 7: the capability for Fowler-Nordheim tunneling is included in a preferred embodiment by Chang et al (col. 5, l. 63+). Furthermore, in reference to the

claim language "may be programmed", intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim, with reference to previously cited case law.

On claim 8: Chang does not necessarily teach the further limitation defined by this claim; however, the thickness of the equivalent of the source /drain diffusion region by Dejenfelt et al falls in the range as witnessed by the cited arsenic implantation energy of 40-60 keV (see, for instance, R. Fair, "Diffusion and Ion Implantation in Silicon", Chapter 7 in "Semiconductor Materials and Process Technology Handbook", Eq. (83) and discussion, from which it is clear that for 60 keV the penetration depth of arsenic (M1=75, Z1=33) in Si (M2=28 and Z2=14) is approximately 0.1 μm. Furthermore, applicant is reminded that it has been held that a *prima facie* case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art or when the ranges of a claimed composition do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. See MPEP 2144.05.

On claim 9: the thickness of the implant in the combined invention includes a range that overlaps with the range as claimed because the voltage of the boron implant in the cited prior art (Dejenfelt et al) ranges from 20 – 40 keV (col. 6, l. 55-57) (see Figs. 9-10(a)-(b) in Wolf (ISBN 0-961672-4-5), showing depth profiles for various voltages for boron implants; cited here for fact, not teaching). Furthermore, applicant is

reminded that it has been held that a *prima facie* case of obviousness typically exists when the ranges of a claimed composition overlap the ranges disclosed in the prior art or when the ranges of a claimed composition do not overlap but are close enough such that one skilled in the art would have expected them to have the same properties. See MPEP 2144.05.

2. ***Claim 4*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al and Dejenfelt et al as applied to claim 1 above, and further in view of and further in view of Chang et al (5,687,118), henceforth called Chang2.

As detailed above, claim 1 is unpatentable over Chang et al in view of Dejenfelt et al. Neither Chang et al nor Dejenfelt et al necessarily teach the further limitation defined by claim 4.

However, it would have been obvious to include said further limitation in view of Chang2, who teach in very closely related art the material constitution of the control gate to be polysilicon as well (cf. col. 11, l. 46-56). *Motivation* to include the teaching by Chang2 at least stems from the economy to use the same material for extremely similar structures in the same invention. Furthermore, Applicant is reminded in this regard that it has been held that mere selection of known materials generally understood to be suitable to make a device, the selection of the particular material being on the basis of suitability for the intended use, would be entirely obvious. See MPEP 2144.07.

3. ***Claim 5*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Chang et al and Dejenfelt et al as applied to claim 1 above, and further in view of Yaegashi et al (US 2002/0098638 A1).

As detailed above, claim 1 is unpatentable over Chang et al in view of Dejenfelt et al. Neither Chang et al nor Dejenfelt et al necessarily teach the further limitation defined by claim 5, although Chang et al do teach the memory cell to include a single polysilicon layer containing a floating gate (col. 4, l. 9-11 and Figure 3).

However it would have been obvious to include said further limitation in view of Yaegashi et al, who teaches a back-gate as control gate to facilitate an operation routinely performed by any memory cell including that of the invention. *Motivation* to include the teaching by Yaegashi et al in the invention thus derives at least from the resulting easier routine performance.

Response to Arguments

Applicant's arguments, see Remarks, filed with aforementioned Amendment with respect to the rejections of claims 1 and 3-9 under 35 USC 103(a) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon further consideration, a new grounds of rejection is made in view of Dejenfelt et al, as included in the rejections provided overleaf.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JPM
October 28, 2007

Primary Patent Examiner:
Johannes Mondt (TC 3600, Art Unit: 3663)